	Application No.	Applicant(s)
Notice of Allowability	09/510,203	FIELDS ET AL.
	Examiner	Art Unit
	Ayal I Sharon	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 10/26/04*.

2. ☒ The allowed claim(s) is/are *1-7 and 9-19*.

3. ☒ The drawings filed on *22 February 2000* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

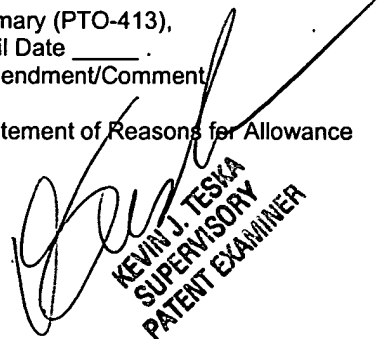   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

    Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____ .

EXAMINER'S AMENDMENT

1. In a telephone interview conducted with the Examiner on 1/31/05, Applicants' Representative, Mr. Kim Kanzaki (Reg. No. 37,652), requested to cancel claims 20-38.

2. Examiner found that these new claims were not supported by arguments pointing out the specific distinctions believed to render the newly presented claims patentable over the applied references, as required under 37 C.F.R. §1.111.

3. In the telephone interview, Applicants' Representative reserved the right to resubmit the claims in a Continuation Application.

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

4. Dependent Claim 8 was indicated as having allowable subject matter in the previous Office Action, dated 7/30/04. In the Amendment that was subsequently filed on 10/26/04, the Applicants amended independent claims 1, 18, and 19 to contain the limitations of claim 8. Claim 8 was cancelled.

5. Claims 1-7 and 9-19 are allowed. The following is an examiner's statement of reasons for allowance for the independent claims: claims 1, 18, and 19.

6. The closest relevant prior art used is:

Bhasker, J., Verilog® HDL Synthesis: A Practical Primer. Chapter 5, "Verification", ©1998. (Henceforth referred to as "**Bhasker**").

7. In regards to Claim 1, Bhasker teaches the following limitations:

> 1.   A computer-implemented method for developing a reusable electronic circuit design module, wherein the design module is comprised of one or more functional design elements

comprising the design module, comprising:

entering the functional design elements into a
database;
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Examiner interprets that the design model and netlists are inherently stored in files, because the synthesis process would not function otherwise.

Examiner interprets that a file fits the dictionary definition of database (see "Claim Interpretations" section in the Office Action dated 7/30/04).

entering documentation elements into the database;
(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Bhasker teaches (p.175) that "Another approach is to write a test bench".

Bhasker's example test bench (pp.175-176) and example functional design element (p.178) contains comment lines. (These lines begin with the "//" symbol).

Examiner interprets that these comments constitute a type of "documentation elements" in the files / "database". (see "Claim Interpretations" section in the Office Action dated 7/30/04).

linking the functional design elements with selected
ones of the documentation elements;
(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Examiner interprets that the embedding of comments in the source code files constitutes a form of "linking" as defined in the dictionary. (see "Claim Interpretations" section in the Office Action dated 7/30/04).

simulating a testbench with the design module, whereby
simulation results are generated;
(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design

model simulation, save the results in a results file and compare to see if the results are identical".

storing the simulation results in the database;
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Bhasker expressly teaches that the simulation results are stored in a results file. Examiner interprets that a file fits the dictionary definition of database (see "Claim Interpretations" section in the Office Action dated 7/30/04).

linking the simulation results with the functional
design elements.
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Examiner interprets that the comparison of the results in the results file (see Fig. 5-2, Fig. 5-3) finds "links" between the simulation results and the functional design elements.

However, Bhasker does not teach or suggest the following limitations in

combination with the above limitations:

inspecting the functional design elements for
associated documentation; and

reporting documentation deficiencies in association
with the functional design elements.

Examiner therefore finds Claim 1, and its dependent claims 2-7 and 9-17 to be

allowable.

8. In regards to Claim 18, Bhasker teaches the following limitations:

> 18.   An apparatus for developing a reusable electronic
> circuit design module, wherein the design module is
> comprised of one or more functional design elements
> comprising the design module, comprising:
>
>   means for entering the functional design elements into
> a database;

(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Examiner interprets that the design model and netlists are inherently stored in files, because the synthesis process would not function otherwise.

Examiner interprets that a file fits the dictionary definition of database (see "Claim Interpretations" section in the Office Action dated 7/30/04).

>   means for entering documentation elements into the
> database;

(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Bhasker teaches (p.175) that "Another approach is to write a test bench".

Bhasker's example test bench (pp.175-176) and example functional design element (p.178) contains comment lines. (These lines begin with the "//" symbol).

Examiner interprets that these comments constitute a type of "documentation elements" in the files / "database". (see "Claim Interpretations" section in the Office Action dated 7/30/04).

>   means for linking the functional design elements with
> selected ones of the documentation elements;

(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Examiner interprets that the embedding of comments in the source code files constitutes a form of "linking" as defined in the dictionary. (see "Claim Interpretations" section in the Office Action dated 7/30/04).

>   means for simulating a testbench with the design
> module, whereby simulation results are generated;

(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

means for storing the simulation results in the.
database; and
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Bhasker expressly teaches that the simulation results are stored in a results file. Examiner interprets that a file fits the dictionary definition of database (see "Claim Interpretations" section in the Office Action dated 7/30/04).

means for linking the simulation results with the
functional design elements.
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Examiner interprets that the comparison of the results in the results file (see Fig. 5-2, Fig. 5-3) finds "links" between the simulation results and the functional design elements.

However, Bhasker does not teach or suggest the following limitations in

combination with the above limitations:

means for inspecting the functional design elements for
associated documentation; and

means for reporting documentation deficiencies in association
with the functional design elements.

Examiner therefore finds Claim 18 to be allowable.

9. In regards to Claim 19, Bhasker teaches the following limitations:

> 19.   A system for developing a reusable electronic circuit
> design module, wherein the design module is comprised of one
> or more functional design elements comprising the design
> module, comprising:
>
>   a database arranged for storage of the design elements
> and documentation elements;

(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.174) that "One approach to verifying functionality is to simulate the netlist with the same set of stimulus as used during design model simulation, save the results in a results file and compare to see if the results are identical".

Bhasker teaches (p.175) that "Another approach is to write a test bench".

Bhasker's example test bench (pp.175-176) and example functional design element (p.178) contains comment lines. (These lines begin with the "//" symbol).

Examiner interprets that these comments constitute a type of "documentation elements" in the files / "database". (see "Claim Interpretations" section in the Office Action dated 7/30/04).

>   a design inspector coupled to the database, the design
> inspector configured and arranged to link the functional
> design elements with selected ones of the documentation
> elements;

(Bhasker, especially: pp.174-175, 178 and Figs. 5-2 and 5-3)

Examiner interprets that the embedding of comments in the design model files constitutes a form of "linking" as defined in the dictionary. (see "Claim Interpretations" section in the Office Action dated 7/30/04).

>   a debugging-support module coupled to the simulator and
> to the database, the debugging-support module configured and
> arranged to generate a netlist from the design module,
> wherein the netlist is suitable for simulation;

(Bhasker, especially: pp.173-175 and Figs. 5-1, 5-2 and 5-3)

Bhasker expressly teaches the use of a "synthesis process" that produces a netlist from a design model. (See Figs. 5-1, 5-2 and 5-3). Bhasker also teaches that the netlist is suitable for simulation (see Figs.5-2 and 5-3)

a functional simulator coupled to the debugging-support
module, the simulator configured and arranged to simulate a
testbench with the design module, whereby simulation results
are generated; and
(Bhasker, especially: p.175 and Fig. 5-3)

Bhasker teaches (p.175) that "Another approach is to write a test bench".

Fig.5-3 shows that a simulator is configured to simulate a testbench with
the design module.

wherein the debugging-support module is further
configured and arranged to store the simulation results in
the database and link the simulation results with the
functional design elements.
(Bhasker, especially: pp.174-175 and Figs. 5-2 and 5-3)

Bhasker teaches (p.175) that "Another approach is to write a test bench; a
test bench is a model written in Verilog HDL that applies stimulus,
compares the output responses, and reports any functional mismatches".

Examiner interprets that a "report" consists of a file, and that the results
inherently link the simulation results with the design elements.

However, Bhasker does not teach or suggest the following limitations in
combination with the above limitations:

inspect the functional design elements for
associated documentation; and

report documentation deficiencies in association
with the functional design elements.

Examiner therefore finds Claim 19 to be allowable.

10. Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should

preferably accompany the issue fee. Such submissions should be clearly labeled

"Comments on Statement of Reasons for Allowance."

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:
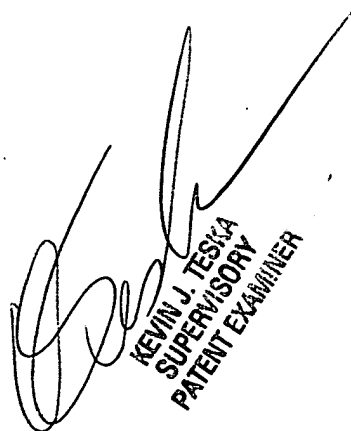
> Director of Patents and Trademarks
> Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

January 31, 2005